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## Question Paper Code: 20356

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Second Semester

Computer Science and Engineering

## CS 6201 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2013)

(Also common to PTCS 6201 – Digital Principles and System Design for B.E. (Part-Time) First Semester — Computer Science and Engineering — Regulations 2014)

Time: Three hours

Maximum: 100 marks

(Codes/ Tables/ Charts to be permitted, if any, may be indicated)

Answer ALL questions.

PART A —  $(10 \times 2 = 20 \text{ marks})$ 

- 1. Convert (7368)<sub>10</sub> into an equivalent binary number.
- 2. List out the advantages and disadvantages of K-map method?
- 3. Mention the design procedure for combinational circuits.
- 4. List any two features of Multiplexer circuit in digital systems.
- 5. What is synchronous counter?
- 6. Give the comparison between combinational circuits and sequential circuits.
- 7. When do race conditions occur?
- 8. Define merger graph.
- 9. List basic types of programmable logic devices.
- 10. State the types of ROM.

## PART B — $(5 \times 16 = 80 \text{ marks})$

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11.	(a)	(i)	Simplify the following Boolean expression to a minimum number of literals. (8)
٠.			AB' + A'C'D' + A'B'D + AB'CD'.
		(ii)	Convert the given expression in canonical SOP form $Y = AC + AB + BC$ . (8)
			Or
	(b)	(i)	List out the procedure for converting Binary to Gray Code. (4)
		(ii)	Convert the following number from one base to other $(65.342)_8 = ()_7$ . (8)
		(iii)	What are the different ways to represent a negative number? (4)
12.	(a)	Expl	ain Logical Implementation of Full-adder and Full-Subtractor. (16)
			Or
	(b)	(i)	Construct 5 to 32 decoder using one 2 to 4 decoder and four 3 to 8 decoder. (6)
	. (1)	(ii)	Design a code converter that converts a decimal digit from 'BCD' code to Excess-3 code. (10)
13.	(a)	: (i)	Explain the working of Master Slave JK Flip Flop. (10)
3	4	(ii)	Discuss about the modification of JK Flip-Flop to form T-FlipFlop with its characteristic table. (6)
			Or
	(b)	(i)	Explain the operation of Serial in Serial out Shift Register. (6)
		(ii)	Design and explain the working of a up down counter. (10)
14.	(a)	_	lain the analysis and design procedures of synchronous sequential uits. (16)
			Or
L/S	(b)		h necessary example and diagram explain the concept of reduction of e and flow tables? (16)

15. (a) Design a 16 bit RAM (4 × 4 RAM) and explain the operation. (16)

Or

(b) Explain the following:

(i) ASIC

(ii) Field Programmable Gate Array. (8)

